Remarks

Claims 1-5 and 10-14 currently stand rejected and remain pending. Claims 6-9 were canceled in a previous response. Claim 12 is amended herein. The Assignee respectfully traverses the rejection and requests allowance of claims 1-5 and 10-14.

Claim Amendments

Claim 12 is amended to improve its grammar and clarity. Thus, no reduction of subject matter or scope of claim 12 is intended.

Claim Rejection Under 35 U.S.C. § 102

Claims 1-5 and 10-14 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 7,036,007 to Schelling et al. (hereinafter "Schelling"). (Page 2 of the Office action.) The Assignee respectfully disagrees as discussed hereinafter.

Independent computer system claim 1 is reproduced below, with emphasis supplied:

> 1. A computer system having a plurality of processors within a cell, the cell comprising:
> a processor type register,
> at least one primary processor;
> *a management subprocessor*,
> an EEPROM, and
> *mapping hardware coupling the plurality of processors to the EEPROM*;
> wherein at system boot the *management subprocessor* reads the processor type register to determine an appropriate boot image of a plurality of boot images recorded within the EEPROM, and *configures the mapping hardware to map the appropriate boot image into boot address space of the at least one primary processor of the cell.*

Independent method claims 2, 13 and 14 provide similar limitations regarding the management subprocessor and the mapping hardware. The Assignee respectfully contends that Schelling does not teach or suggest at least the subprocessor and the mapping hardware set forth in the independent claims.

The Office action indicates that Schelling discloses both the management subprocessor and the mapping hardware mentioned above. More specifically, the Office action states that "col. 3, lines 34-37; col. 4, lines 3-7, 26-54; cited columns and lines clearly indicate there is an

intelligence that that is implemented as a management subprocessor to find, search, and/or locate a processor-specific firmware component(s)." (Pages 3, 4, 5 and 6 of the Office action.) Additionally, the Office action indicates that Schelling teaches the mapping hardware at "col. 4, line 26 -- col. 5, line 36; col. 7, lines 30-37; mapping via vector location (e.g., address) and entry points." (Pages 3, 4, 6 and 7 of the Office action.) The Assignee respectfully disagrees.

Generally, Schelling discloses "a firmware architecture which splits firmware modules to support safe updates of specific modules as well as supporting multiple different processors." (Abstract.) To this end, boot-up or restart firmware is organized into separate generic or non-processor-specific modules executable by all processor types, and processor-specific modules. (See Fig. 2; and column 3, line 44, to column 4, line 15.) The processor being booted or restarted then (1) begins executing the firmware at its reset vector, (2) jumping to and executing generic Processor Abstraction Layer (PAL) components, (3) searching for, jumping to, and executing processor-specific PAL components, (4) jumping to and executing generic System Abstraction Layer (SAL) components, and (5) searching for, jumping to, and executing processor-specific SAL components. (See Fig. 3; and column 4, line 16, to column 5, line 36.) To facilitate the searching and jumping functions, the processor may consult a firmware interface table (FIT) containing entries identifying the various processor-specific modules and their entry points. (Column 4, line 50, to column 5, line 7; and column 5, lines 23-28.) Fig. 4 graphically displays the typical attributes of the modules and pointers described above. (See also column 5, line 38, to column 7, line 50.)

Thus, the various embodiments described in Schelling are distinguished from the subject matter of claims 1, 2, 13 and 14 in several ways. For one, the processor being booted or restarted in Schelling performs all of the searching, locating and executing of processor-specific firmware modules, contrary to the assertions of the Office action. For example, Fig. 3 shows how the rebooted processor begins execution at its reset vector, and then searches for and executes the various generic and processor-specific modules (operations 302-320), as described above. Moreover, Schelling does not mention a management processor or subprocessor at all, as provided for in claims 1, 2, 13 and 14.

Further, Schelling does not teach or suggest reading a processor type register to determine an appropriate boot image from a plurality of boot images, and configure mapping hardware to map that boot image into boot address space of a processor, as set forth in claims 1,

2, 13 and 14. Rather, Schelling specifically indicates that "the different aspects of the embodiments of the invention described, permit supporting multiple processors with *a single firmware image*." (Column 8, lines 13-15; emphasis supplied.) Since a single firmware image is employed, Schelling does not employ or mention multiple such images. In addition, the firmware image of Schelling is configured so that the reset vector of the processor "jumps to a PAL entry point 302" to begin the reboot process. (See column 4, lines 26-29, referring to Fig. 3.) Thus, Schelling does not teach or suggest mapping its single boot image into boot address space of that processor, as the image is already located at the appropriate place in the address space. As a result, Schelling does not require, teach or suggest mapping hardware for performing such a function, as provided in claims 1, 2, 13 and 14.

Thus, based on the foregoing, the Assignee contends that claims 1, 2, 13 and 14 are allowable in view of Schelling, and such indication is respectfully requested.

Claims 3-5 and 10-12 depend from independent claim 2, thus incorporating the provisions of that independent claim. Thus, the Assignee asserts that claims 3-5 and 10-12 are allowable for at least the reasons provided above in support of claim 2, and such indication is respectfully requested.

Therefore, in light of the above, the Assignee respectfully requests withdrawal of the 35 U.S.C. § 102 rejection of claims 1-5 and 10-14.

Conclusion

Based on the above remarks, the Assignee submits that claims 1-5 and 10-14 are allowable. Other reasons in favor of patentability exist, but such reasons are omitted in the interests of clarity and brevity. The Assignee thus respectfully requests allowance of claims 1-5 and 10-14.

The Assignee believes no fees are due with respect to this filing. However, should the Office determine additional fees are necessary, the Office is hereby authorized to charge Deposit Account No. 08-2025 accordingly.

Respectfully submitted,

Date: 5/2/07

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